A Silicon Bipolar Technology for High-Efficiency Power Applications up to *C*-Band

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***Abstract* — This paper presents the large-signal characterization and modeling of a 0.8-μm 46-GHz-f_T silicon bipolar technology for RF power applications up to *C*-band. A series of devices with optimized layout and vertical structure was fabricated for on-wafer load-pull testing at 1.9 GHz, 2.4 GHz, and 5.2 GHz. Under continuous-wave operation, a 56% power-added efficiency and 11-dB large-signal gain were achieved at a 22-dBm output power level by an 80-μm emitter length device (180-μm^2 emitter area) operating at 5.2 GHz with a 2.7-V supply voltage. A modified Gummel-Poon model was extracted from DC and multibias *S*-parameter measurements and validated by comparisons with load-pull results. Close agreement was found between simulated and measured large-signal performance up to power levels well above the 1-dB compression point.**

I. Introduction

Future generation wireless communication standards will require ever higher operating frequencies for faster data transmission rate and increasing number of users. At the same time, the low-voltage and high-efficiency requirements will still hold for battery-operated mobile handsets to allow extended operating time and small equipment size. Currently, the power amplifier market is dominated by III-V semiconductor technologies because they can provide excellent performance in meeting such requirements. However, the high cost and low thermal conductivity of these materials make them unfit for higher integration levels. For this reason, the prospect of an efficient RF power amplifier in conventional low-cost Si-based technology has been attracting increasing attention over the last few years. Despite recent efforts [1-3], efficiency values higher than 50% have not yet been reported for pure silicon bipolar power transistors operating up to *C*-band.

In this work, the low-voltage power capabilities of a high-performance low-cost silicon bipolar process were explored by harmonic source/load-pull measurements up to 5.2 GHz. Proper device layout and vertical structure design resulted in the excellent power-added efficiency (PAE) of 56% at 5.2 GHz with a supply voltage as low as 2.7 V. Moreover, close agreement was also achieved between measured and simulated large-signal characteristics up to saturated-output power levels by using a modified Gummel-Poon model.

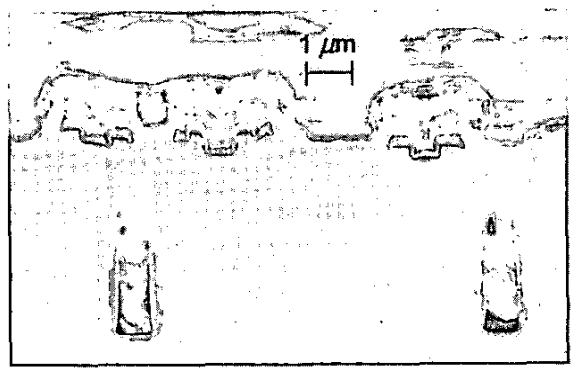

Figure 1. SEM cross-section of a 0.8-μm bipolar transistor.

TABLE I
BJT TYPICAL PERFORMANCE PARAMETERS
(0.8×8 μm^2 mask-level emitter area)

h_{FE}	180
V_A [V]	28
f_T [GHz] (V_{CB} = 2 V)	46
f_{max} [GHz] (V_{CB} = 2 V)	54
NF_{min} [dB] (f = 2 GHz)	0.8
BV_{CEO} [V]	3.4
BV_{CBO} [V]	16
BV_{EBO} [V]	2

II. Device Design and Performance

The devices were fabricated in a 46-GHz-f_T 0.8-μm three-metal-layer self-aligned-emitter silicon bipolar process by STMicroelectronics (BiPMOS). This is a low-cost technology requiring only 19 mask steps. Oxide trench is used to provide low-parasitic lateral isolation of

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active devices. This technology also allows a p-channel MOSFET to be included as a complementary device so that bias and control functions can be accurately implemented. The technology also provides two poly resistor layers, MIM capacitors (0.7 fF/μm^2), and varactors. The third metal layer (3-μm-thick AlSiCu) is used for on-chip spiral inductors with Q values up to 10 at 2 GHz and resonant frequencies above 15 GHz. Figure 1 shows a SEM cross-section of a 0.8-μm-emitter transistor. Typical electrical performance of bipolar devices is outlined in Table I.

A series of test devices was fabricated and characterized at 1.9 GHz (L-band), 2.4 GHz (S-band), and 5.2 GHz (C-band), in accordance with commercial frequency bands.

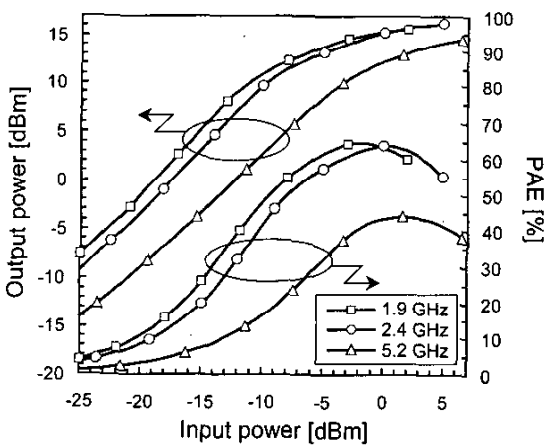

Figure 2. Output power and PAE versus input power for the 10-μm transistor (V_{CC} = 2.7 V, I_Q = 1 mA, harmonic load-pull CW test).

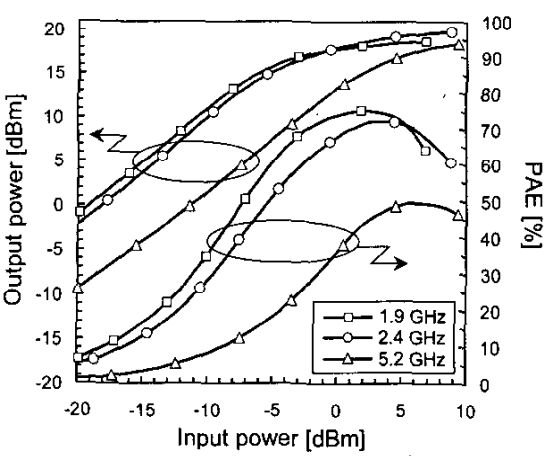

Figure 3. Output power and PAE versus input power for the 30-μm transistor (V_{CC} = 2.7 V, I_Q = 3 mA, harmonic load-pull CW test).

A spot-emitter layout was adopted to better exploit the emitter perimeter. The mask-level spot size was set to 0.8 μm × 2 μm. In addition, a reduced epi-layer thickness of 0.8 μm was adopted for high-efficiency low-voltage operation [4]. Four transistors with different emitter lengths were integrated to test the effects of current crowding along the emitter metal finger (10 μm, 30 μm, 50 μm, and 80 μm). On-wafer harmonic source/load-pull measurements were carried out with a 2.7-V supply voltage using a single-tone continuous-wave (CW) input. Harmonic load impedances were tuned for maximum PAE (dual-Class-F operation [5]). The same quiescent current density was set for each of the transistors being tested. A quiescent collector current of 1 mA was set for the 10-μm device and proportionally increased for longer ones.

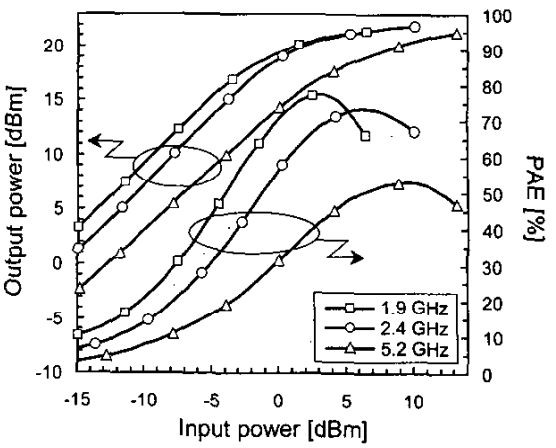

Figure 4. Output power and PAE versus input power for the 50-μm transistor (V_{CC} = 2.7 V, I_Q = 5 mA, harmonic load-pull CW test).

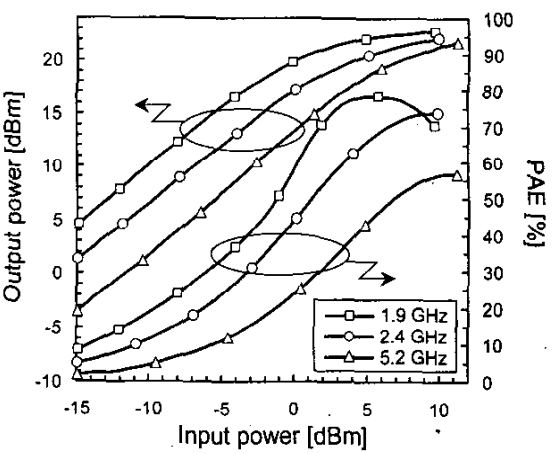

Figure 5. Output power and PAE versus input power for the 80-μm transistor (V_{CC} = 2.7 V, I_Q = 8 mA, harmonic load-pull CW test).

The output power and PAE characteristics versus input power are plotted in Figures 2 through 5 for each emitter length and test frequency with a 2.7-V power supply. A peak efficiency of 79% was achieved at 1.9 GHz and a record PAE of 56% was reached at 5.2 GHz by the 80-μm transistor (see Figure 5). The 5.2-GHz power performance of the four test devices is summarized for comparison in Figures 6 and 7.

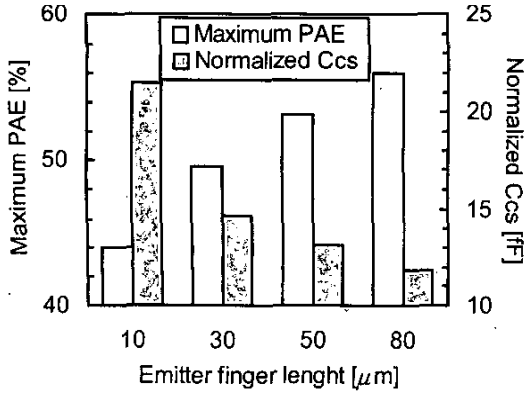

Figure 6. Maximum PAE and normalized Ccs versus emitter finger length at 5.2 GHz (V_{CC} = 2.7 V, harmonic load-pull CW test).

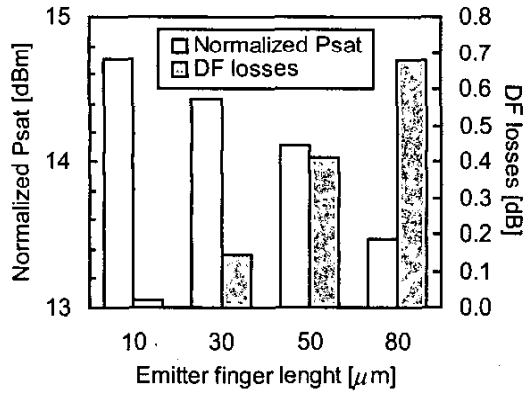

Figure 7. Normalized P_{SAT} and DF losses versus emitter finger length at 5.2 GHz (V_{CC} = 2.7 V, harmonic load-pull CW test).

The PAE improves as emitter length increases since perimeter capacitive parasitics at the collector node are proportionally larger in shorter transistors than in longer ones. This is confirmed by measurements of the zero-bias collector-substrate junction capacitance obtained from "cold device" S parameters (normalized to a 10-μm emitter length in Figure 6). The 80-μm transistor had a 44% less normalized collector-substrate capacitance than the 10-μm one, thereby allowing 12% more maximum PAE. On the other hand, the saturated output power decreases as the emitter length increases due to the current capability degradation occurring in longer transistors, which is caused by the voltage drop across the distributed resistance of emitter metal fingers. A simple and accurate expression for the DC degradation factor up to medium current levels is provided in [6]. Taking into account only the first-order term of such expression, losses associated with the "average" degradation factor for large-signal continuos-wave operation (expressed in dB) can be calculated using the following formula:

$$DF_{losses} \approx -10 \cdot \log_{10}\left(1 - \frac{R_E \cdot I_E}{3 \cdot V_T}\right) \qquad (1)$$

where I_E is the average emitter current at the saturated output power level. The resistance of emitter metal fingers (R_E) can be calculated using the following formula, which also takes into account the increase in resistivity due to skin effect at 5.2 GHz:

$$R_E = R_{SH} \cdot \frac{L_E}{W_E} \cdot \frac{t}{\delta \cdot (1 - e^{-t/\delta})} \qquad (2)$$

where δ is the skin depth at 5.2 GHz while R_{SH}, L_E, W_E and t are the sheet resistance, length, width and thickness of the emitter metal fingers, respectively. The saturated output power P_{SAT} (normalized to a 10-μm emitter length) and the degradation factor losses are shown in Figure 7 for each emitter length. Given that a first-order approximation was used to calculate DF losses and that errors of tenths of dB can affect the measurement of saturated output power, it can be concluded that current capability degradation is responsible for most of the power losses occurring in longer transistors.

III. LARGE-SIGNAL MODELING

Accurate large-signal modeling is of paramount importance for the design of highly nonlinear circuits, such as power amplifiers. In this work, an ST-SPICE Gummel-Poon model was adopted [7]. Still maintaining the same basic formulation of the standard Gummel-Poon model, it features additional parameters and equations taking into account only the most important second-order effects (i.e., Kirk effect, avalanche breakdown, temperature-dependent model parameters). Therefore, the main limitations of the standard Gummel-Poon model can be overcome with a minimum increase in complexity. Model parameters were extracted from measured DC and *S*-parameters. The high-current region of the forward *I-V* curves was exploited to extract base push-out parameters.

The model accuracy for non-linear operation was investigated by comparison with on-wafer large-signal load-pull measurements. Simulated and measured output power, PAE and power gain for the 50-μm transistor

(optimum source and load impedances) are shown in Figures 8 through 10. The curves displayed reveal an excellent agreement between predicted and experimental performance, although no model parameter optimization was carried out to improve the large-signal fitting. At any test frequency, the maximum error on the output power and power gain is lower than 0.6 dB over the entire input power range, whereas the peak PAE is predicted with a better than 4% accuracy.

IV. Summary

The potential of a high-performance low-cost silicon bipolar technology for high-frequency efficient RF power amplifiers was explored. To this end, a set of test devices with optimized layout and vertical structure was fabricated for on-wafer load-pull characterization at 1.9 GHz, 2.4 GHz, and 5.2 GHz. Several emitter finger lengths were considered to investigate the compromise between PAE and output power density. Efficiency values up to 79% were achieved at 1.9 GHz and 2.7 V supply voltage. Moreover, a very high PAE of 56% was obtained at 5.2 GHz. A modified Gummel-Poon model yielded good agreement between simulated and measured power characteristics. These results set a record for the power performance of silicon bipolar technology. They show that a pure silicon process is a promising choice for low-cost high-volume fabrication of efficient power amplifiers up to *C*-band.

Acknowledgement

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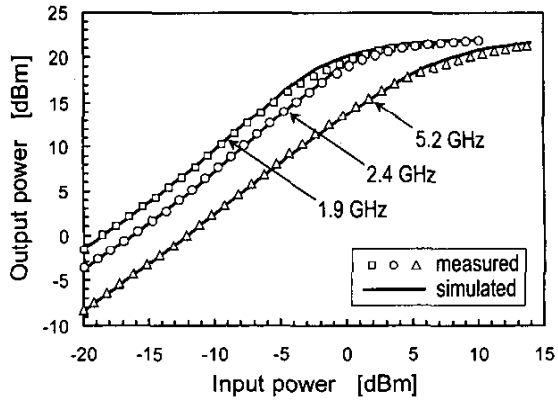

Figure 8. Simulated and measured output power versus input power for the 50-μm transistor (V_{CC} = 2.7 V, I_Q = 5 mA).

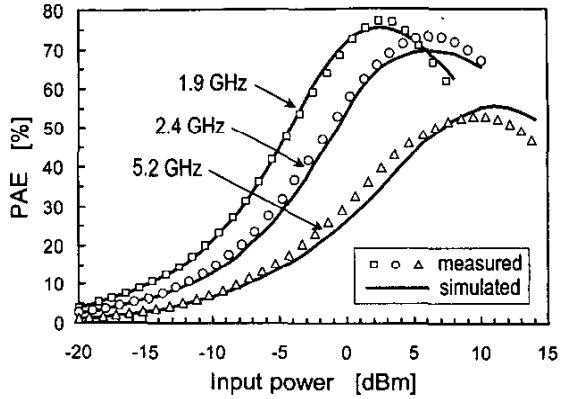

Figure 9. Simulated and measured PAE versus input power for the 50-μm transistor (V_{CC} = 2.7 V, I_Q = 5 mA).

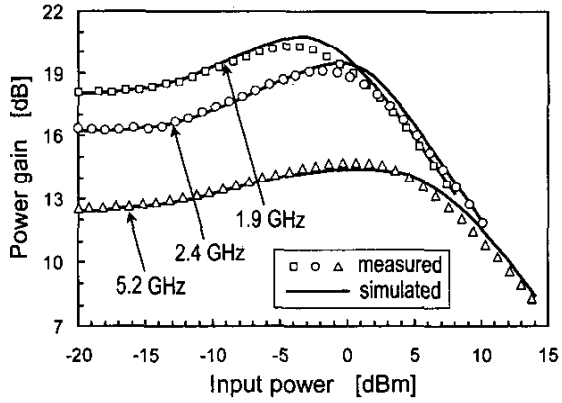

Figure 10. Simulated and measured power gain versus input power for the 50-μm transistor (V_{CC} = 2.7 V, I_Q = 5 mA).